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G06F 17/50 // H03K 19/177

(52) UK CL (Edition R)
G4H HU H13D

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GB 2305528 A

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(54) Abstract Title
Implementing logic circuits

(57) A programmable monolithic integrated logic circuit includes look up table circuits and programmable logic array-like circuits. The integrated circuit can include a first number of the look up tables and a second number of the programmable logic array-like circuits and where the first and second numbers are related by a ratio of between 0.25:1 and 6:1, between 1:1 and 5:1, or about 4:1. The programmable logic array-like circuits can each include at least 10,000 or 50,000 equivalent two-input NAND gates and the look up tables and the programmable logic array-like circuits can each comprise static random access cells. A method of implementing a logic circuit includes reading a netlist that includes a plurality of subnets, determining the suitability of ones of the subnets to being implemented with look up tables and with programmable logic array-like circuits, and determining whether to implement each subnet with a look up table or a programmable logic array-like circuit based on results of the step of determining. Based on the steps of determining, the method implements a first subnet of the plurality of subnets with look up table circuits and a second subset of the plurality of subnets with programmable logic array-like circuits.

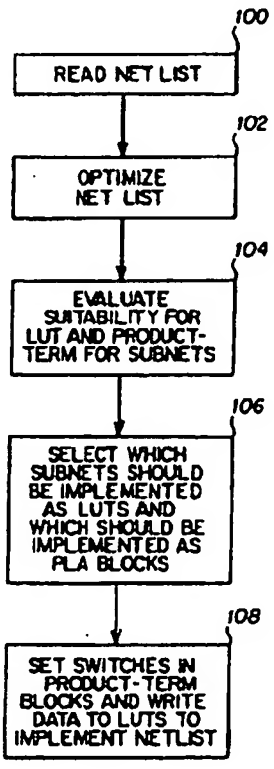

FIG. 6

GB 2 345 369 A

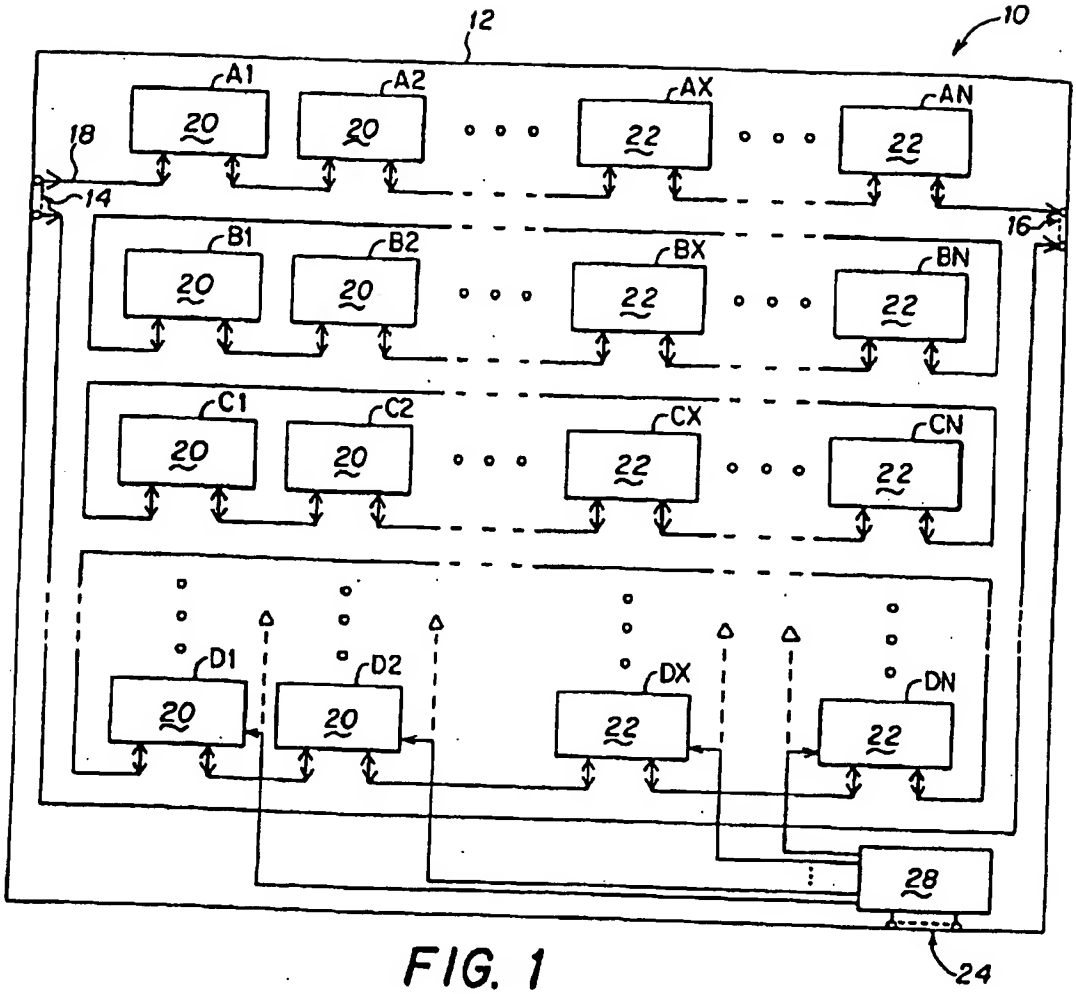
12
10
A1
A2
AX
AN
18
14
16
B1
B2
BX
BN
C1
C2
CX
CN
D1
D2
DX
DN
20
22
28
24

FIG. 1

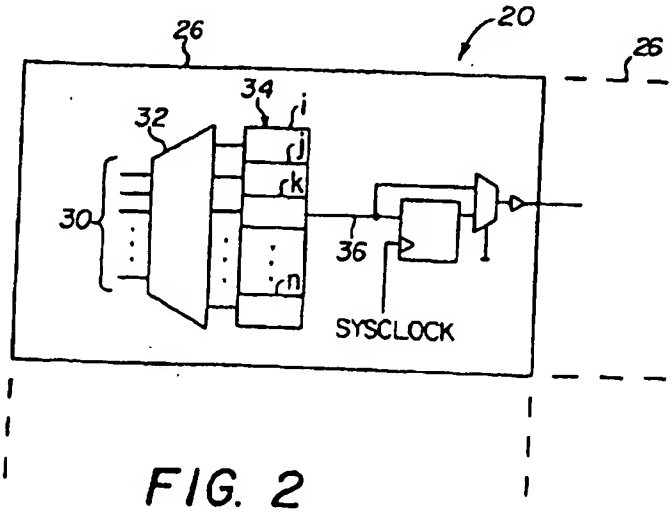
26
20
26
34
i
32
j
k
30
n
36
SYSCLOCK

FIG. 2

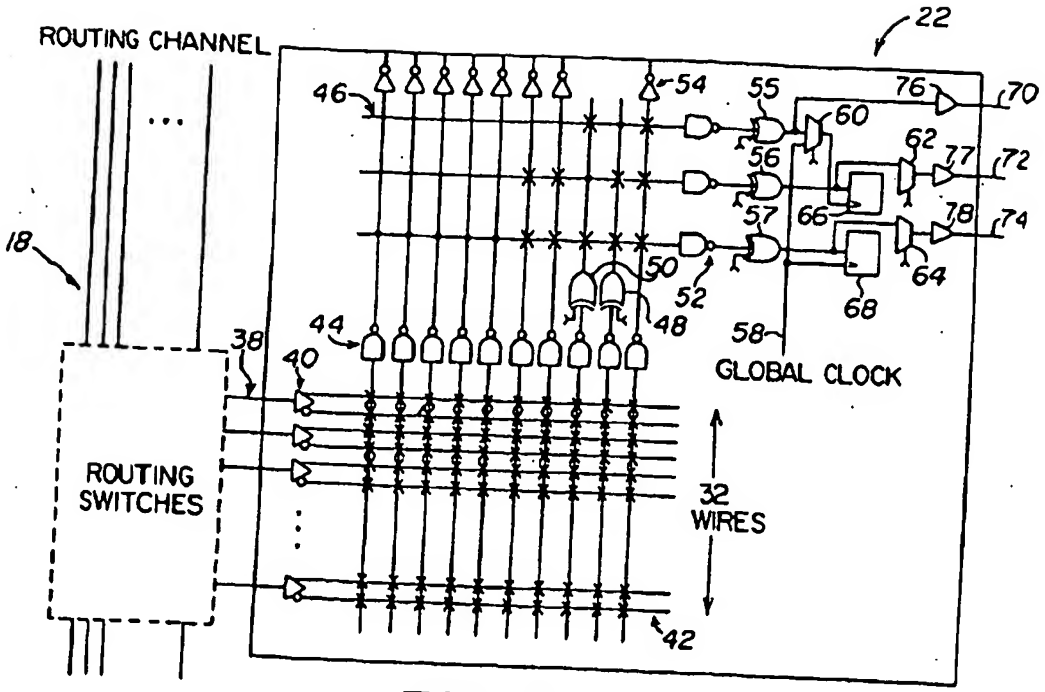

FIG. 3

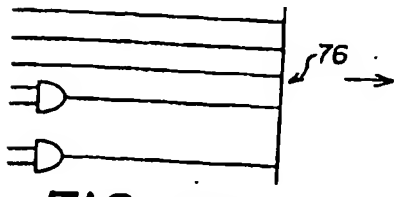

FIG. 4A

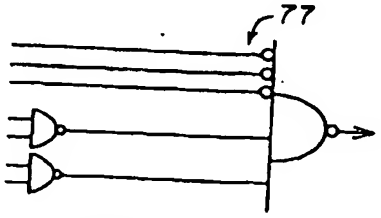

FIG. 4B

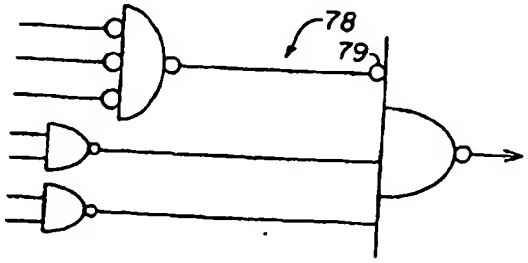

FIG. 4C

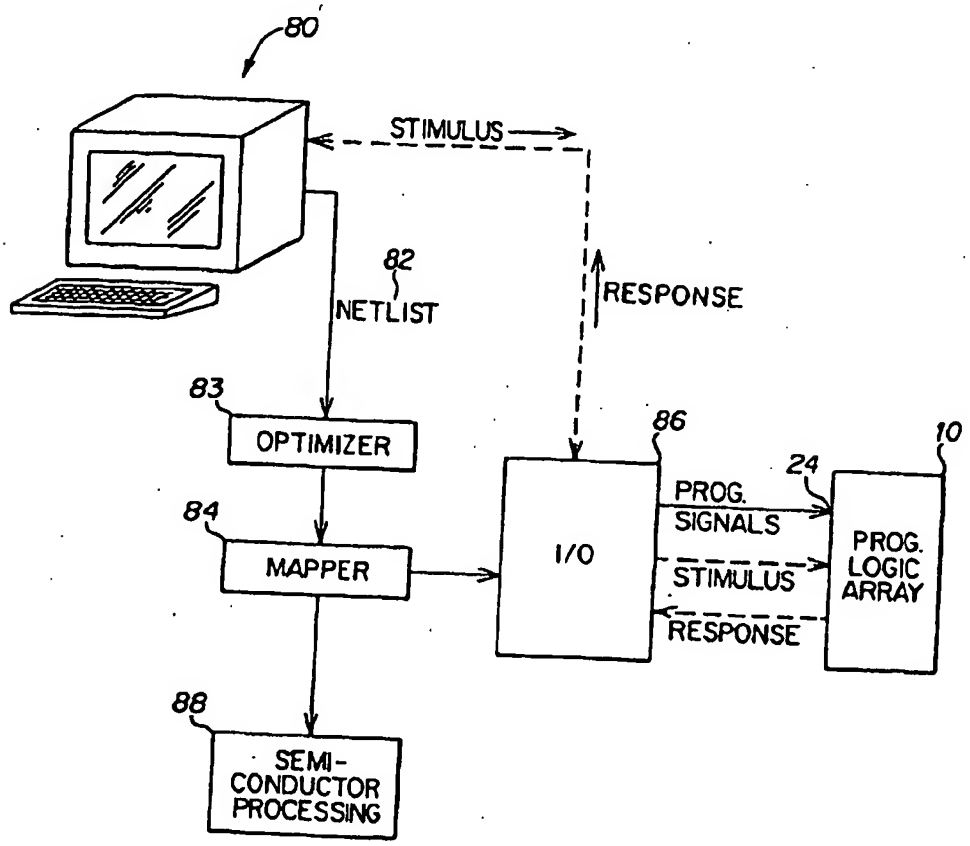
80
STIMULUS
82
NETLIST
RESPONSE
83
OPTIMIZER
86
10
24
84
MAPPER
I/O
PROG.
SIGNALS
STIMULUS
RESPONSE
PROG.
LOGIC
ARRAY
88
SEMI-
CONDUCTOR
PROCESSING

FIG. 5

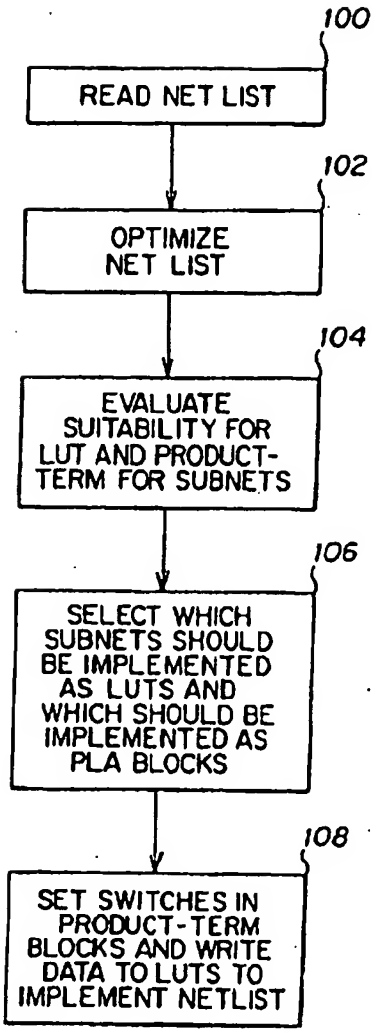
100
READ NET LIST
102
OPTIMIZE NET LIST
104
EVALUATE SUITABILITY FOR LUT AND PRODUCT-TERM FOR SUBNETS
106
SELECT WHICH SUBNETS SHOULD BE IMPLEMENTED AS LUTS AND WHICH SHOULD BE IMPLEMENTED AS PLA BLOCKS
108
SET SWITCHES IN PRODUCT-TERM BLOCKS AND WRITE DATA TO LUTS TO IMPLEMENT NETLIST

FIG. 6

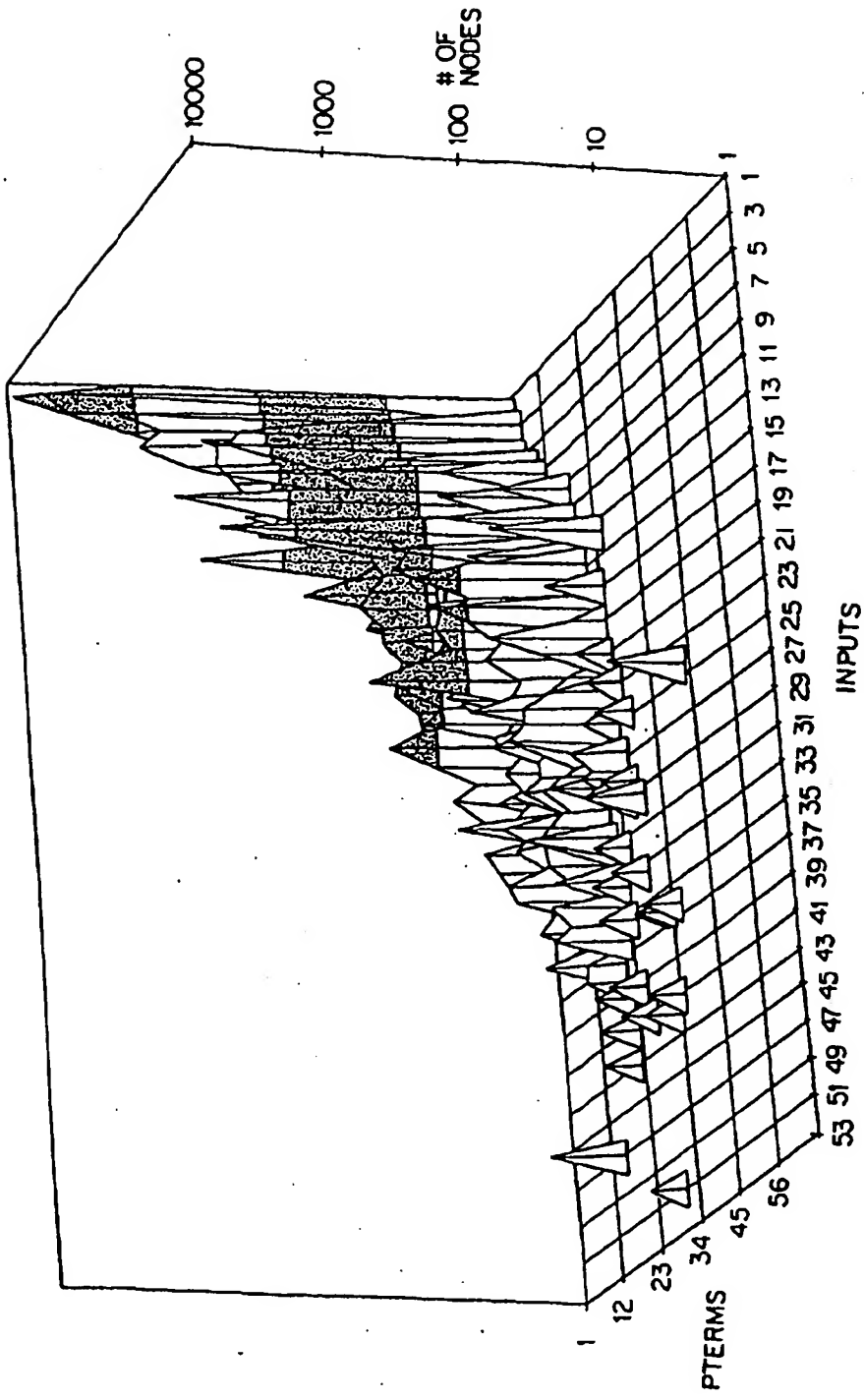
OF NODES
10000
1000
100
10
1
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49 51 53
INPUTS
1 12 23 34 45 56
PTERMS

FIG. 7

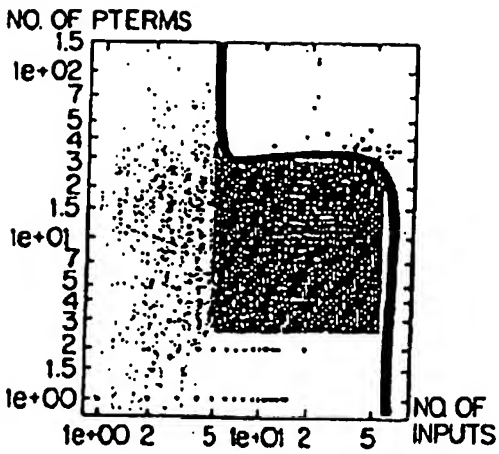

FIG. 8

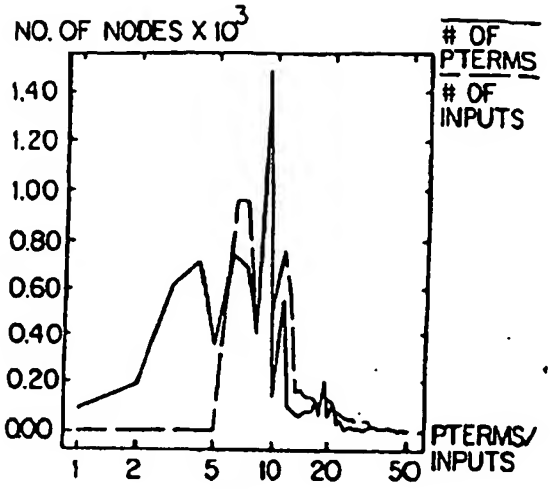

FIG. 9

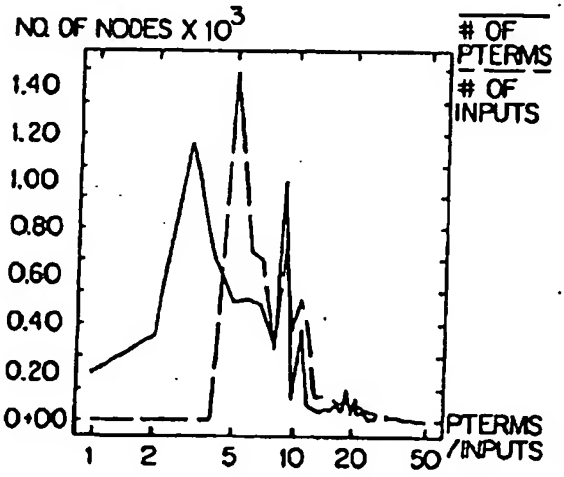

FIG. 10

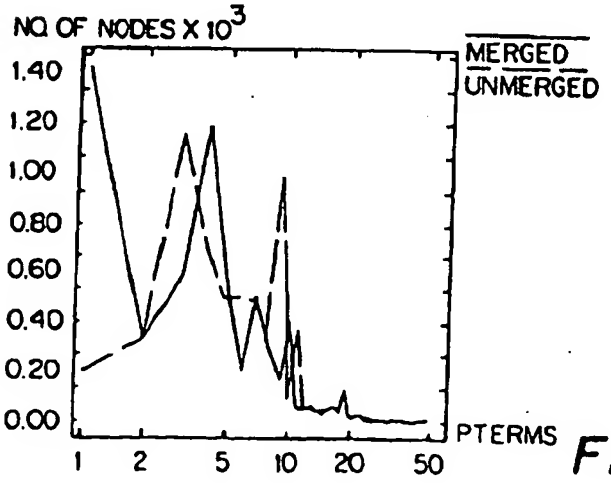

FIG. 11